CLAIMS:

1. A time cycle suppressor circuit for use with delay locked loops, said time cycle suppressor circuit comprising:

an input node for receiving an input signal;

an inverter circuit, said inverter circuit operationally coupled to said input node for providing a complement to said input signal;

a first latch circuit, said first latch circuit having an input for receiving said input signal, a reset input for resetting said first latch circuit, a data input operationally connected to a voltage source, and a first output signal;

a second latch circuit, said second latch circuit having an input for receiving said complement to said input signal, a reset input for resetting said second latch circuit, a data input operationally connected to said first output signal, and a second output signal;

a first AND gate having a first input and a second input, wherein said first input is operationally connected to said first output signal, and said second input is operationally connected to said second output signal, said first AND gate having a third output signal;

a second AND gate having a first input and a second input, wherein said first input is operationally connected to said third output signal, and said second input is operationally connected to said complement to said input signal, said second AND gate having a fourth output signal; and

an output node for outputting said fourth output signal.

2. The time cycle suppressor circuit of claim 1, wherein said first latch circuit and said second latch circuit are D-flipflops.

3. The time cycle suppressor circuit of claim 2, wherein said input signal is a reference clock signal.

4. The time cycle suppressor circuit of claim 3, wherein said reference clock signal has a period T.

5. The time cycle suppressor circuit of claim 4, wherein said fourth output signal begins at a time, wherein said time is a fraction of the period T of the reference clock signal.

6. The time cycle suppressor circuit of claim 5, wherein said fourth output signal begins at a time approximately equal to T/2.

7. A method for conditioning with a time cycle suppressor circuit, for use with delay locked loops, said method comprising:

providing an input node for receiving an input signal;

providing an inverter circuit, said inverter circuit operationally coupled to said input node for providing a complement to said input signal;

providing a first latch circuit, said first latch circuit having an input for receiving said input signal, a reset input for resetting said first latch circuit, a data input operationally connected to a voltage source, and a first output signal;

providing a second latch circuit, said second latch circuit having an input for receiving said complement to said input signal, a reset input for resetting said second latch circuit, a data input operationally connected to said first output signal, and a second output signal;

providing a first AND gate having a first input and a second input, wherein said first input is operationally connected to said first output signal, and said second input is operationally connected to said second output signal, said first AND gate having a third output signal;

providing a second AND gate having a first input and a second input, wherein said first input is operationally connected to said third output signal, and said second input is operationally connected to said complement to said input signal, said second AND gate having a fourth output signal; and

providing an output node for outputting said fourth output signal.

8. The time cycle suppressor circuit of claim 7, wherein said first latch circuit and said second latch circuit are D-flipflops.

9. The time cycle suppressor circuit of claim 8, wherein said input signal is a reference clock signal.

10. The time cycle suppressor circuit of claim 9, wherein said reference clock signal has a period T.

11. The time cycle suppressor circuit of claim 10, wherein said fourth output signal begins at a time, wherein said time is a fraction of the period T of the reference clock signal.

12. The time cycle suppressor circuit of claim 11, wherein said fourth output signal begins at a time approximately equal to T/2.

13. A DLL circuit architecture for reducing lock time in said DLL, said DLL circuit architecture comprising:

an input node for receiving an input signal, wherein said input signal is a reference clock signal having a period;

a time cycle suppressor circuit, said time cycle suppressor circuit operationally coupled to said input node;

a phase frequency detector circuit operationally coupled to said time cycle suppressor circuit;

a charge pump circuit operationally coupled to said phase frequency detector circuit;

a coarse delay tuner circuit, said coarse delay tuner circuit operationally coupled to said input node;

a fine delay tuner circuit, said fine delay tuner circuit operationally coupled to said coarse delay tuner circuit and to said phase frequency detector; and

an output node operationally coupled to said fine delay tuner circuit, for outputting a fine delay output signal.

14. The DLL circuit architecture of claim 13, wherein said time cycle suppressor circuit is adapted to condition said input signal, and to provide a first output signal having a delay equal to a fraction of said period of said reference clock signal.

15. The DLL circuit architecture of claim 13, wherein said phase frequency detector circuit is adapted to receive said first output signal from said time cycle suppressor circuit, said phase frequency detector circuit is adapted to provide at least one control signal to said charge pump circuit, and wherein said phase frequency detector circuit has a second input adapted to receive a second input signal.

16. The DLL circuit architecture of claim 15, wherein said charge pump circuit includes a low pass filter to condition said control signal, and wherein said charge pump circuit provides a control output signal.

17. The DLL circuit architecture of claim 13, wherein said a coarse delay tuner circuit is operationally coupled to said input node, and wherein said coarse delay tuner circuit is adapted to produce a coarse delay output signal which has a starting point approximately equal to a fraction of said period of said reference clock signal.

18. The DLL circuit architecture of claim 15, wherein said fine delay tuner circuit is operationally coupled to said coarse delay tuner circuit, wherein said fine delay tuner circuit removes errors from said coarse delay output signal and produces a fine delay output signal, wherein said fine delay tuner circuit is additionally operationally coupled to said charge pump circuit for receiving said control signal from said charge pump circuit, and wherein said fine delay output signal is outputted to said second input of said phase frequency detector.

19. A method for reducing lock time in a delay locked loop (DLL), said method comprising:
providing an input node for receiving an input signal, wherein said input signal is a reference clock signal having a period;

providing a time cycle suppressor circuit, said time cycle suppressor circuit operationally coupled to said input node;

providing a phase frequency detector circuit operationally coupled to said time cycle suppressor circuit;

providing a charge pump circuit operationally coupled to said phase frequency detector circuit;

providing a coarse delay tuner circuit, said coarse delay tuner circuit operationally coupled to said input node;

providing a fine delay tuner circuit, said fine delay tuner circuit operationally coupled to said coarse delay tuner circuit and to said phase frequency detector; and

providing an output node operationally coupled to said fine delay tuner circuit, for outputting a fine delay output signal.

20. The DLL circuit architecture of claim 19, wherein said time cycle suppressor circuit is adapted to condition said input signal, and to provide a first output signal having a delay equal to a fraction of said period of said reference clock signal.

21. The DLL circuit architecture of claim 19, wherein said phase frequency detector circuit is adapted to receive said first output signal from said time cycle suppressor circuit, said phase frequency detector circuit is adapted to provide at least one control signal to said charge pump circuit, and wherein said phase frequency detector circuit has a second input adapted to receive a second input signal.

22. The DLL circuit architecture of claim 21, wherein said charge pump circuit includes a low pass filter to condition said control signal, and wherein said charge pump circuit provides a control output signal.

23. The DLL circuit architecture of claim 19, wherein said a coarse delay tuner circuit is operationally coupled to said input node, and wherein said coarse delay tuner circuit is adapted to produce a coarse delay output signal which has a starting point approximately equal to a fraction of said period of said reference clock signal.

24. The DLL circuit architecture of claim 19, wherein said fine delay tuner circuit is operationally coupled to said coarse delay tuner circuit, wherein said fine delay tuner circuit removes errors from said coarse delay output signal, and produces a fine delay output signal, wherein said fine delay tuner circuit is additionally operationally coupled to said charge pump circuit for receiving said control signal from said charge pump circuit, and wherein said fine delay output signal is outputted to said second input of said phase frequency detector.

25. A semiconductor device with a synchronous memory component utilizing a DLL, said semiconductor device comprising:

a reference clock signal applied to said synchronous memory device at an input node;

a time cycle suppressor circuit, said time cycle suppressor circuit operationally coupled to said input node;

a phase frequency detector circuit operationally coupled to said time cycle suppressor circuit;

a charge pump circuit operationally coupled to said phase frequency detector circuit;

a coarse delay tuner circuit, said coarse delay tuner circuit operationally coupled to said input node;

a fine delay tuner circuit, said fine delay tuner circuit operationally coupled to said coarse delay tuner circuit and to said phase frequency detector circuit; and

an output node operationally coupled to said fine delay tuner circuit, for outputting a fine delay output signal.

26. The semiconductor device of claim 25, wherein said time cycle suppressor circuit is operationally coupled to said input node, wherein said time cycle suppressor circuit is adapted to condition said input signal, and to provide a first output signal having a delay equal to a fraction of said period of said reference clock signal.

27. The semiconductor device of claim 25, wherein said phase frequency detector circuit is adapted to receive said first output signal from said time cycle suppressor circuit, said phase frequency detector circuit is adapted to provide at least one control signal to said charge pump circuit, and wherein said phase frequency detector circuit has a second input adapted to receive a second input signal.

28. The semiconductor device of claim 27, wherein said charge pump circuit including a low pass filter to condition said control signal, wherein said charge pump circuit provides a control output signal.

29. The semiconductor device of claim 25, wherein said a coarse delay tuner circuit is operationally coupled to said input node, wherein said coarse delay tuner circuit is adapted to produce a coarse delay output signal which has a starting point approximately equal to a fraction of said period of said reference clock signal.

30. The semiconductor device of claim 27, wherein said fine delay tuner circuit is operationally coupled to said coarse delay tuner circuit, wherein said fine delay tuner circuit removes errors from said coarse delay output signal, and produces a fine delay output signal, wherein said fine delay tuner circuit is additionally operationally coupled to said charge pump circuit for receiving said control signal from said charge pump circuit, and wherein said fine delay output signal is outputted to said second input of said phase frequency detector.

31. A method for reducing lock time in a delay locked loop (DLL) in a semiconductor device with a synchronous memory component utilizing a DLL, said method comprising:

providing an input node for receiving an input signal, wherein said input signal is a reference clock signal having a period;

providing a time cycle suppressor circuit, said time cycle suppressor circuit operationally coupled to said input node;

providing a phase frequency detector circuit operationally coupled to said time cycle suppressor circuit;

providing a charge pump circuit operationally coupled to said phase frequency detector circuit;

providing a coarse delay tuner circuit, said coarse delay tuner circuit operationally coupled to said input node;

providing a fine delay tuner circuit, said fine delay tuner circuit operationally coupled to said coarse delay tuner circuit and to said phase frequency detector; and

providing an output node operationally coupled to said fine delay tuner circuit, for outputting a fine delay output signal.

32. The method of claim 31, wherein said time cycle suppressor circuit is operationally coupled to said input node, wherein said time cycle suppressor circuit is adapted to condition said input signal, and to provide a first output signal having a delay equal to a fraction of said period of said reference clock signal.

33. The method of claim 31, wherein said phase frequency detector circuit is adapted to receive said first output signal from said time cycle suppressor circuit, said phase frequency detector circuit is adapted to provide at least one control signal to said charge pump circuit, and wherein said phase frequency detector circuit has a second input adapted to receive a second input signal.

34. The method of claim 33, wherein said charge pump circuit including a low pass filter to condition said control signal, wherein said charge pump circuit provides a control output signal.

35. The method of claim 31, wherein said a coarse delay tuner circuit is operationally coupled to said input node, wherein said coarse delay tuner circuit is adapted to produce a coarse delay output signal which has a starting point approximately equal to a fraction of said period of said reference clock signal.

36. The method of claim 33, wherein said delay tuner circuit is operationally coupled to said coarse delay tuner circuit, wherein said fine delay tuner circuit removes errors from said coarse delay output signal, and produces a fine delay output signal, wherein said fine

delay tuner circuit is additionally operationally coupled to said charge pump circuit for receiving said control signal from said charge pump circuit, and wherein said fine delay output signal is outputted to said second input of said phase frequency detector.

37. An apparatus containing a synchronous integrated circuit, said apparatus comprising:

a synchronous memory component;

a reference clock signal applied to said synchronous memory component; and

a delay locked loop, wherein said delay locked loop includes circuit architecture for reducing lock time in said synchronous memory component, said circuit architecture further comprising:

an input node for receiving an input signal, wherein said input signal is a reference clock signal having a period;

a time cycle suppressor circuit, said time cycle suppressor circuit operationally coupled to said input node;

a phase frequency detector circuit operationally coupled to said time cycle suppressor circuit;

a charge pump circuit operationally coupled to said phase frequency detector circuit;

a coarse delay tuner circuit, said coarse delay tuner circuit operationally coupled to said input node;

a fine delay tuner circuit, said fine delay tuner circuit operationally coupled to said coarse delay tuner circuit and to said phase frequency detector; and

an output node operationally coupled to said fine delay tuner circuit, for outputting a fine delay output signal.